storing a new state metric of the initial state of the trellis in a respective initial state register as soon as the respective initial state of the trellis has been stored in the buffer register.--

Remarks:

This preliminary amendment is being submitted in an effort to correct informalities and provide improved translations of certain wording in the initial application, and to present claims in proper U.S. claims idiom and to remove multiple dependencies. The changes are not made for any reason related to the statutory requirements for a patent nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent. The newly entered claims are fully supported in the original claims.

The recommended subheadings have been inserted at the proper locations in the text.

New FIGS. 2 and 4 of the drawings are submitted for approval. Specifically, functional blocks in FIGS. 2 and 4 have been given labels.

All of the changes are properly supported in the original application. No new matter has been added.

An early action on the merits of the application is solicited.

The fee for seven (7) additional claims in excess of twenty (20) pursuant to Section 1.16 in the amount of $126.00 is enclosed herewith. Applicants note that the fee for one additional claim in excess of twenty (20) was already paid.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants
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Version of Specification With Markings to Show Changes Made:

Replace the paragraphs beginning on lines 7, 10, and 12 of page 1, with:

--Background of the Invention:

Field of the Invention:

Such an apparatus and such a method are [known from [1]] disclosed in WO 99/34520, corresponding to U.S. Patent NO. 6,115,436 to Ramesh et al. (hereinafter "Ramesh").

In the method [known from [1]] and [in the] apparatus [known from [1]] disclosed in Ramesh, a received decoded signal is decoded by [means of] an electrical circuit that is disposed [which is arranged] in accordance with a so-called butterfly structure. [This known] The Ramesh procedure is used exclusively for channel decoding of channel-coded signals.--.

Replace the paragraphs beginning on lines 1, 11, 16, 18, and 23 of page 2, with:

--[[2]] W. Koch and A. Baier, Optimum and Suboptimum Detection of Coded Data Disturbed by Time-Varying Intersymbol Interference, IEEE GLOBECOM, pages 1679 - 1684, 1999 (hereinafter "Koch"), discloses the determination of a so-called transition metric for a Viterbi algorithm in the course of equalization of physical signals for so-called soft decision equalization. Furthermore, [[2]] Koch discloses the entire Viterbi method, matched to the appropriate transition

metrics for a so-called butterfly structure of a trellis, and the determination of the "optimum" signal sequence of the received signals by [means of] so-called back-tracing from the optimum trellis determined.

One particular disadvantage of the procedure described in Koch [[2]] is that the circuit described there is suitable only for equalization of received physical signals. The Koch apparatus cannot be used for channel decoding of physical signals.

The principles of the Viterbi algorithm are described in [[3]] G.D. Forney, The Viterbi-Algorithm, Proceedings of the IEEE, Vol., 61, No. 3, pages 268 - 278, 1973 (hereinafter "Forney").

Summary of the Invention:

It is accordingly an object of the invention to provide a device and method to carry out a veterbi algorithm that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices of this general type and that makes [The invention is thus based on the problem of making] it possible to use a Viterbi algorithm flexibly for different, selectable operating modes, for example, for equalization and for decoding received physical signals.--

Replace the paragraphs beginning on page 12, lines 5, 7, 9, 12, 15, 20, and 24 with:

--Brief Description of the Drawings:

[An exemplary embodiment of the invention will be explained in more detail in the following text and is illustrated in the figures, in which:

Figure 1 shows an exemplary embodiment of an electrical circuit according to the invention;]

Fig. 1 is a block circuit diagram of an exemplary embodiment of an electrical circuit according to the invention;

[Figure 2 shows a block diagram, illustrating the sending, transmission and reception of an electrical signal;]

Fig. 2 is a block circuit diagram illustrating the sending, transmission, and reception of an electrical signal;

[Figures 3a and 3b show a sketch illustrating a binary trellis according to a butterfly structure for equalization (Figure 3a) and for decoding (Figure 3b) of an electrical signal;]

Fig. 3A is a diagram illustrating a binary trellis according to a butterfly structure for equalization of an electrical signal;

Figs. 3B is a diagram illustrating a binary trellis according to a butterfly structure for decoding an electrical signal; and

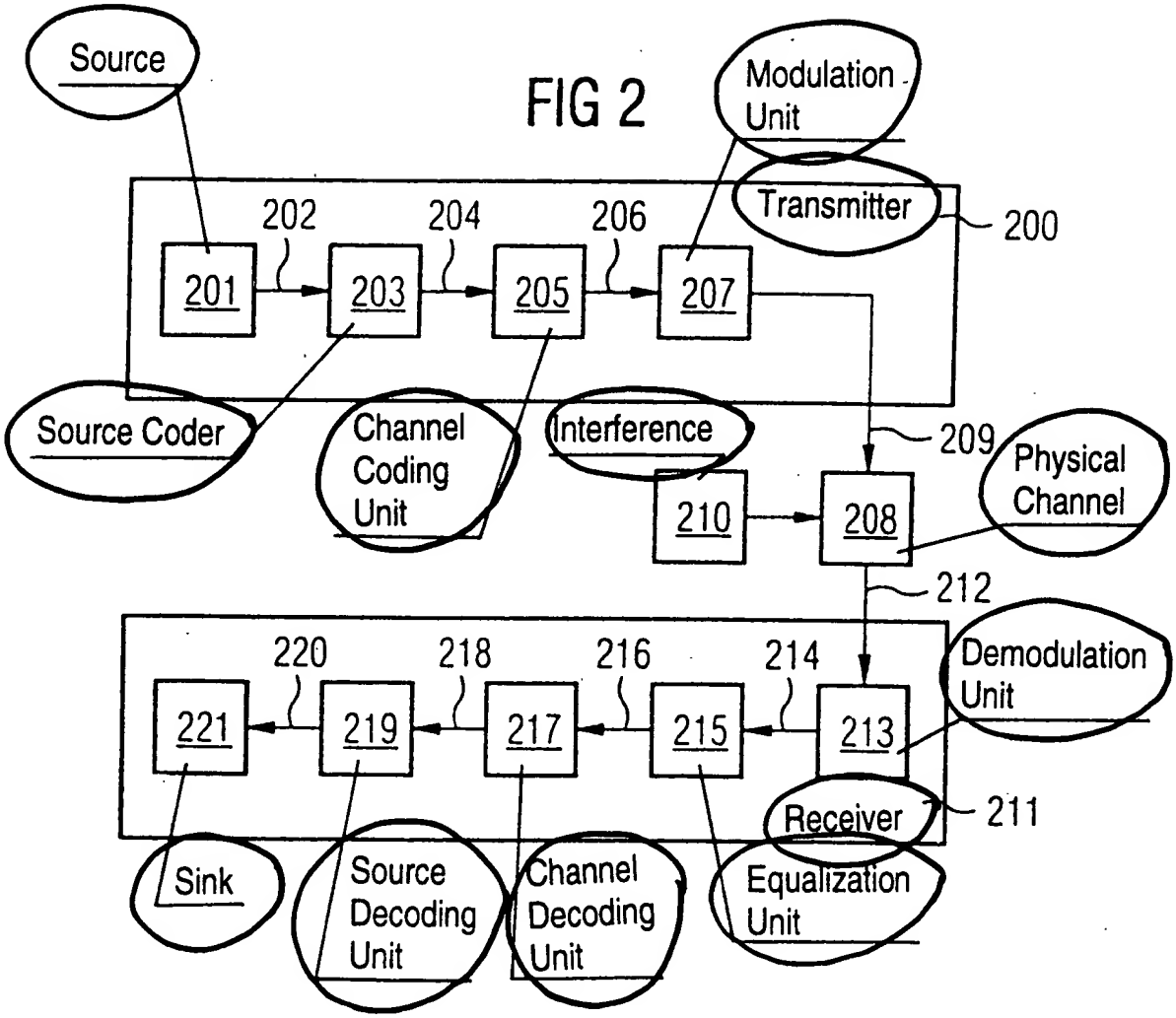
[Figure 4 shows a block diagram of an exemplary embodiment of a digital signal processor according to the invention.]
Fig. 4 is a block circuit diagram of an exemplary embodiment of a digital signal processor according to the invention.

Description of the Preferred Embodiments:

Referring now to the figures of the drawings in detail and first, particularly to Fig. 2 thereof, there is shown, [Figure 2 shows,] symbolically, a source 201, from which a message 202 is intended to be transmitted from a transmitter 200 to a sink 221 in a receiver 211.--.

Replace the paragraphs beginning on page 17, line 14, with:
--To simplify understanding of the invention, the rough structure of the Viterbi algorithm will be explained in the following text (see Figure 3A [3a] and Figure 3B [3b]). Details of the Viterbi algorithm are described in Fourny [[3]].--.

FIG 2


Source
Modulation Unit
Transmitter
200
202
204
206
201
203
205
207
Source Coder
Channel Coding Unit
Interference
209
Physical Channel
210
208
212
220
218
216
214
Demodulation Unit
221
219
217
215
213
Receiver
211
Sink
Source Decoding Unit
Channel Decoding Unit
Equalization Unit

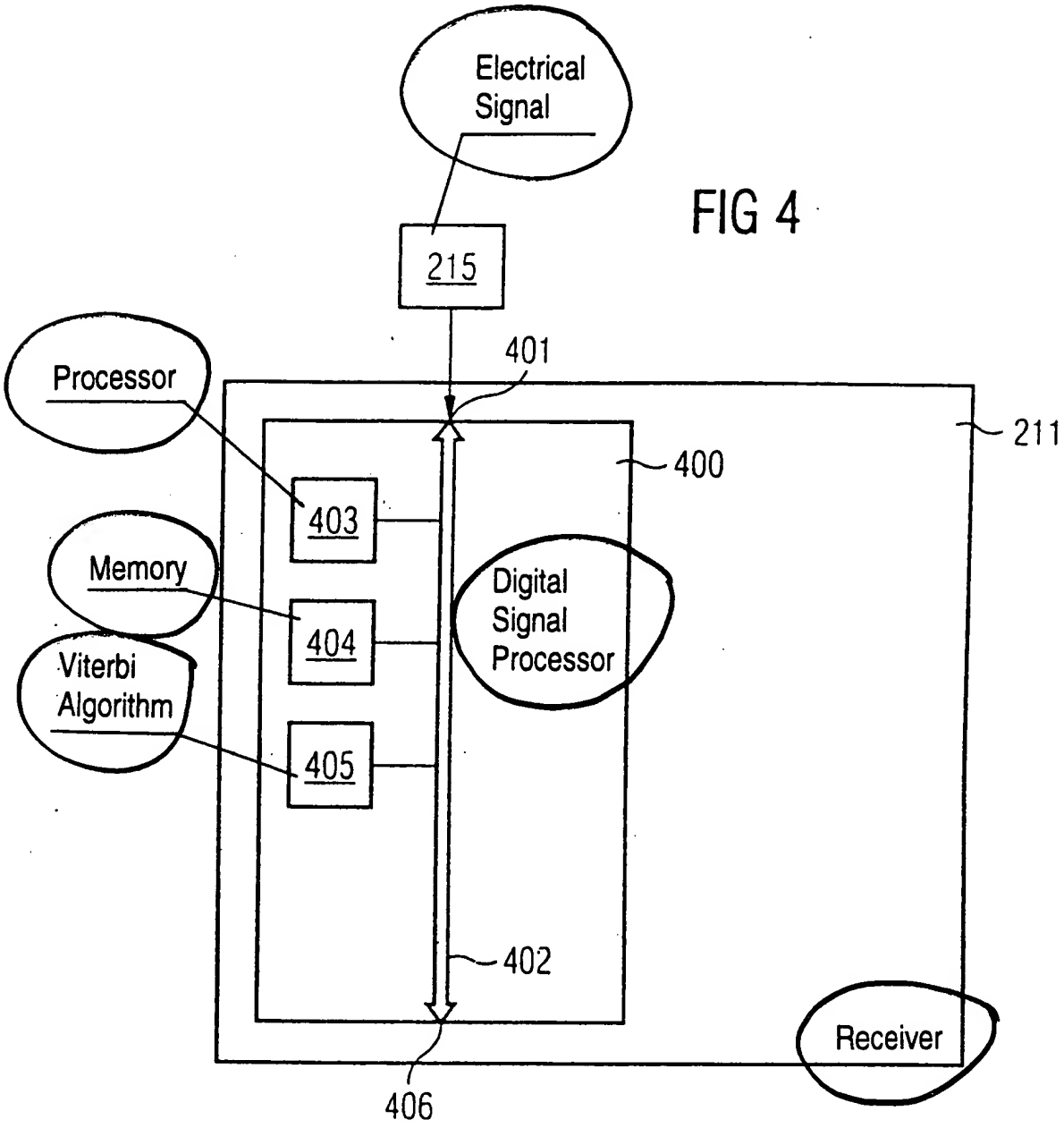

Electrical Signal
215
401
Processor
211
400
403
Memory
404
Digital Signal Processor
Viterbi Algorithm
405
402
Receiver
406

FIG 4